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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,523	06/27/2001	Ryan N. Rakvic	2207/1123601	3187

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,523	RAKVIC ET AL.	
	Examiner	Art Unit	
	Midys Inoa	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-18,20-23,26-28 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,10,12,14-18,20-23,26-28 and 30-33* is/are rejected.

7)☒ Claim(s) *11 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/31/04, 5/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9-10, 12, 14-18, and 26-28, are rejected under 35 U.S.C. 102(e) as being anticipated by Rappoport et al. (6,549,987).

Regarding Claim 10, Rappoport discloses cache assignment method, comprising:

receiving plural data request ("separate address signal for each of the banks", Column 3, lines 51-59),

each associated with respective cachelet pointers (Column 3, lines 51-59 and Column 4, lines 44-60) **wherein a cache line is addressed and accessed (data requests) using a "set" and a bank vector (or cachelet pointer) and instruction segment associate the "set" to the individual bank. Therefore, as a set selects an entry within a bank, in making that selection, it is also selecting a bank;**

determining whether any of the cachelet pointers conflict with any other cachelet pointers through a comparison of cachelet pointers (bank vectors) which reveals an overlap or conflict of pointers (Column 5, lines 28-51),

if a conflict occurs among cachelet pointers, forwarding one of the data requests associated with a conflicting cachelet pointer to the identified cachelet, wherein this cachelet pointer belongs to the first pointer in the order of the program flow,

and deferring the remaining data request with the conflicting cachelet pointer; **wherein deferring the request, it is essentially being reassigned to an unused cachelets since the action of deferring it has the effect of allowing the access to take place once the cachelet is no longer in use.**

Regarding Claim 9, Rapoport discloses a cache assignment method further comprising forwarding any data requests associated with non-conflicting cachelet pointers to cachelets (banks) identified by the respective pointers (Column 5, lines 15-26).

Regarding Claim 14, Rappoport discloses cache assignment method, comprising:

receiving plural data request ("separate address signal for each of the banks", Column 3, lines 51-59),

each associated with respective cachelet pointers (Column 3, lines 51-59 and Column 4, lines 44-60) **wherein a cache line is addressed and accessed (data requests) using a "set" and a bank vector (or cachelet pointer) and instruction segment associate the "set" to the individual bank. Therefore, as a set selects an entry within a bank, in making that selection, it is also selecting a bank;**

determining whether any of the cachelet pointers conflict with any other cachelet pointers through a comparison of cachelet pointers (bank vectors) which reveals an overlap or conflict of pointers (Column 5, lines 28-51),

if a conflict occurs among cachelet pointers, forwarding one of the data requests associated with a conflicting cachelet pointer to the identified cachelet, wherein this cachelet pointer belongs to the first pointer in the order of the program flow,

and deferring the remaining data request with the conflicting cachelet pointer; **wherein deferring the request, it is essentially being reassigned to an unused cachelets since the action of deferring it has the effect of allowing the access to take place once the cachelet is no longer in use**

the method further comprising forwarding any data requests associated with non-conflicting cachelet pointers to cachelets (banks) identified by the respective pointers (Column 5, lines 15-26).

Regarding Claims 12, 15-18 and 26-28, Rappoport discloses a cache assignment method, comprising:

receiving plural data requests ("separate address signal for each of the banks", Column 3, lines 51-59)

and associated cachelet pointers addressing one of a plurality of cachelets within a cache (Column 3, lines 51-59 and Column 4, lines 44-60) **wherein a cache line is addressed and accessed (data requests) using a "set" and a bank vector (or cachelet pointer) and instruction segment associate the "set" to the individual bank. Therefore, as a set selects an entry within a bank, in making that selection, it is also selecting a bank** (see also Figure 3), determining whether any of the cachelet pointers are valid ("a comparison determines that if no overlap is present, the pointers are valid"), forwarding data requests having valid cachelet pointers to the addressed cachelet ("there is no overlap... retrieving both instructions from the

cache" Column 5, lines 5-33), and assigning remaining data requests (invalid or conflicting requests) to unused cachelets according to a default assignment scheme, wherein the scheme involves forwarding the first data requests in the program flow order to the identified cachelet, and deferring the remaining data request with the conflicting cachelet pointer; **wherein deferring the request, it is essentially being reassigned to an unused cachelets since the action of deferring it has the effect of allowing the access to take place once the cachelet is no longer in use.**

Claims 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Rappoport et al. (6,549,987) and The Authoritative Dictionary of IEEE Standards Terms, wherein The Authoritative Dictionary is used as an evidentiary reference.

Regarding Claims 20 and 22, Rappoport discloses a cache system comprising: a first layer of cache (cache memory 230, Figure 2), comprising a plurality of independently addressable cachelets (banks 310, Figure 3) and means for distributing multiple loads among the cachelets in a single clock cycle ("retrieve data in a single clock cycle", Column 5, lines 27-30), and a second layer of cache (segment cache 280, Figure 2) to receive a load that misses the cachelet to which it was assigned (data is supplied by either the instruction cache or the segment cache, Column 3, lines 4-37 and the selector 290 selects the output from ether cache). Since the data is supplied by either one of the cache layers, when the first cache memory layer cannot supply the data, the second segment cache memory layer must receive the missed request. The Authoritative Dictionary discloses an instance in which in disk caching, a hit occurs when the targeted data is located in a first level of cache storage, and thus there is no need to reference

secondary storage. However, when the targeted data is not present, secondary storage must be referenced (Page 519),

Regarding Claims 21 and 23, the instruction cache #210 of Rappoport can be a system memory since it is part of a system (Figure 2).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rappoport et al. (6,549,987).

Regarding Claims 30-33, Rappoport et al. teaches the invention as set forth by Claims 10 and 14 above. Rappoport et al. does not teach forwarding the reassigned data requests in parallel with the other forwarded data requests. It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the invention of Rappoport et al. to forward reassigned commands in parallel to other commands since the system already has the ability to address the memory banks independently from one another during the same clock cycle (in other words, it has the ability to address memory banks in parallel) and extending this parallel ability to the reassigned requests would allow for these requests to be processed faster and more efficiently.

Response to Arguments

4. Applicant's arguments filed May 17th, 2004 have been fully considered but they are not persuasive.

Applicant argues that Rappoport teaches selecting an entry within a bank, not among banks. **The system of Rappoport addresses and accesses (data requests) a cache line using a "set"; a bank vector (or cachelet pointer) and instruction segment associate the "set" to the individual bank. Therefore, as a set selects an entry within a bank, in making that selection, it is also selecting a bank from the plurality of banks.**

Applicant argues that Rappoport does not teach reassigning remaining conflicting cachelet pointers to unused cachelets. However, Rappoport teaches deferring the remaining data request with the conflicting cachelet pointer; **wherein deferring the request, it is essentially being reassigned to an unused cachelets since the action of deferring it has the effect of allowing the access to take place once the cachelet is no longer in use.**

Allowable Subject Matter

5. Claims 11 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claim 11, the Prior Art of Record does not teach multiple data requests having common set addresses being forwarded to different cachelets. Unlike the claimed invention, the invention of Rappoport discloses instruction segments with common overlapping addresses causing a conflict as they are forwarded to the same bank (or cachelets). The limitation of claim 11 does not appear to be found in the Prior Art of record.

Regarding Claim 13, the Prior Art of Record does not teach storing copies of a single data item in multiple cachelets. The invention of Rappoport does not teach any of the banks acting as a mirror for another bank. Further more, the prior art does not teach a traditional cache architecture allowing the storage of redundant copies of data. The limitation of claim 13 does not appear to be found in the Prior Art of record.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa

Midys Inoa
Examiner
Art Unit 2188

MI

Mano Padmanabhan 9/7/04

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SUPERVISORY PATENT EXAMINER